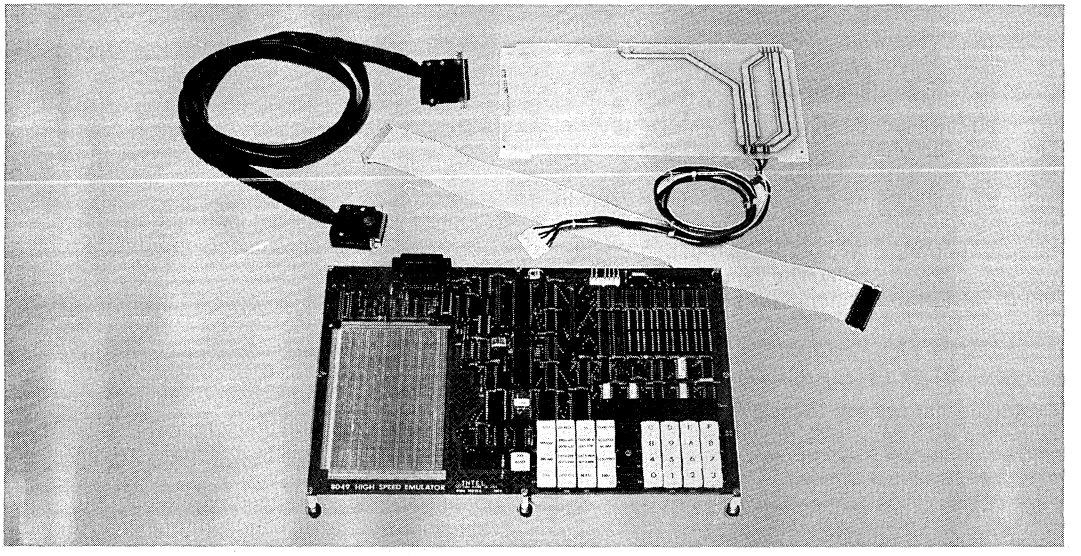
HSE-49
HIGH-SPEED EMULATOR

- **Single-board execution and debugging vehicle with integral keypad and display**
- **System monitor firmware in ROM**
- **Wire-wrap area for prototyping**
- **Intellec®-system compatible power pick-up card and serial-link cable**
- **Real-time 11 MHz emulation of user system**
- **Breakpoints on user program and external data addresses**
- **Examine and alter MCS® -48 registers, memory and status values**
- **No-break triggering of oscilloscope or logic analyzer**

The HSE-49™ emulator is a fully-assembled stand-alone development tool with on-board 33-key keypad, 8-character display, two 8039 microcontrollers, 2K bytes of user-program RAM, a serial port and cable, and a ROM-based monitor which supervises the emulator operation and user interface. The emulator provides a means for executing and debugging programs for the 8048/8049 family of microcontrollers at speeds up to 11 MHz. It interfaces to a user-designed system through an emulation cable and 40-pin plug, which replaces the MCS-48™device in the user's system. Using the HSE-49 keypad, a designer can run programs in real-time or single-step modes, set up to 8000 breakpoint flags, and display or change the contents of user program memory, internal and external data memory, and internal MCS-48 hardware registers. When linked to a host Intellec® development system, the HSE-49 emulator system-debugging capabilities, with the development system program assembly and storage facilities, provide the tools required for total product development.



FUNCTIONAL DESCRIPTION

The HSE-49 High-Speed Emulator is a stand-alone execution and debugging tool for 8048/8049 family microcontroller-based systems which are designed to run at speeds up to 11 MHz. It may be used alone or with other Intel microcomputer development system products to facilitate system integration early in the product development cycle, in parallel with hardware and software development. The convenient two-way debugging which early integration permits results in reduced total development time and cost.

System Development

SOFTWARE DEVELOPMENT

After an application program has been written in MCS-48 assembly language, the HSE-49 emulator may be used to debug software even if prototype hardware is not yet available.

Stand-alone Mode

The designer first hand assembles the source code from ASM-48 mnemonics into hex code, and then loads the program into the HSE-49 emulator user-program RAM through the on-board hex keypad, or through the serial port from a hex file stored on a user-supplied peripheral device. The emulator may then be used to execute the user program in a variety of debugging modes, and to alter the program as necessary. The altered program may then be uploaded to a user-supplied storage device.

Development System Mode

With an Intellec development system, the designer assembles the source code using the MCS-48 macroassembler and downloads the resulting hex file through the serial port and cable to the HSE-49 emulator user-program RAM. The emulator is then used to execute and debug the program as above. Finally, the resulting program is uploaded to the development system and stored in a disk file.

HARDWARE/SOFTWARE INTEGRATION

Prototype hardware may be developed off-board or on the wire-wrap area provided on the HSE-49 emulator board. The HSE-49 emulator interfaces to the user-system hardware through the supplied emulation cable, which plugs into the MCS-48 device socket in the user system. With the plug in place, the emulator executes code from the user-program memory and exercises the prototype hardware. Additional hardware is added as it becomes available, and the system is debugged using the emulator's capabilities to break emulation and to examine and change the user program and processor status values. The completed system may be final tested prior to ROM-code entry by replacing the HSE-49 emulation plug with a programmed 874X device in the user-system MCS-48 device socket, and running the system (with crystal input and power supplied) at full speed. Figure 1 shows a typical development configuration utilizing a host Intellec development system and the HSE-49 emulator, with the emulation cable interface to a user-designed system.

For enhanced system debugging capabilities the designer may elect to use Intel's ICE-49™ in-circuit emulator. The ICE-49 module permits real-time emulation of the user system up to 6 MHz, and offers the added benefits of symbolic debugging, 255 instruction-cycle real-time trace, and full emulation without the stack, interrupt or I/O limitations to which the HSE-49 emulator is subject (see discussion under "Limitations" heading). For further information on the ICE-49 emulator, refer to the ICE-49™ In-Circuit Emulator Data Sheet (order number 305200).

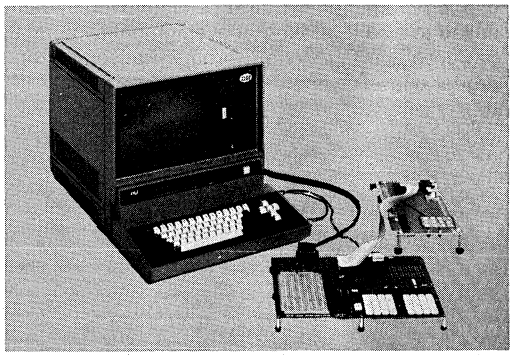


Figure 1. Intellec® System Based HSE-49 Emulator Connected to User Prototype System

Emulator Overview

EMULATION AND MASTER PROCESSORS

The user's program is emulated by an 8039 microprocessor, the emulation processor (EP), which executes code that is stored in 2K bytes of external RAM for ease of program development. Additional RAM may be added by the user in the provided sockets to expand program and external data memory to 4K bytes each.

A second microcontroller — an 8039 with off-chip ROM program memory — is used to scan the on-board keypad and display, interpret and imple-

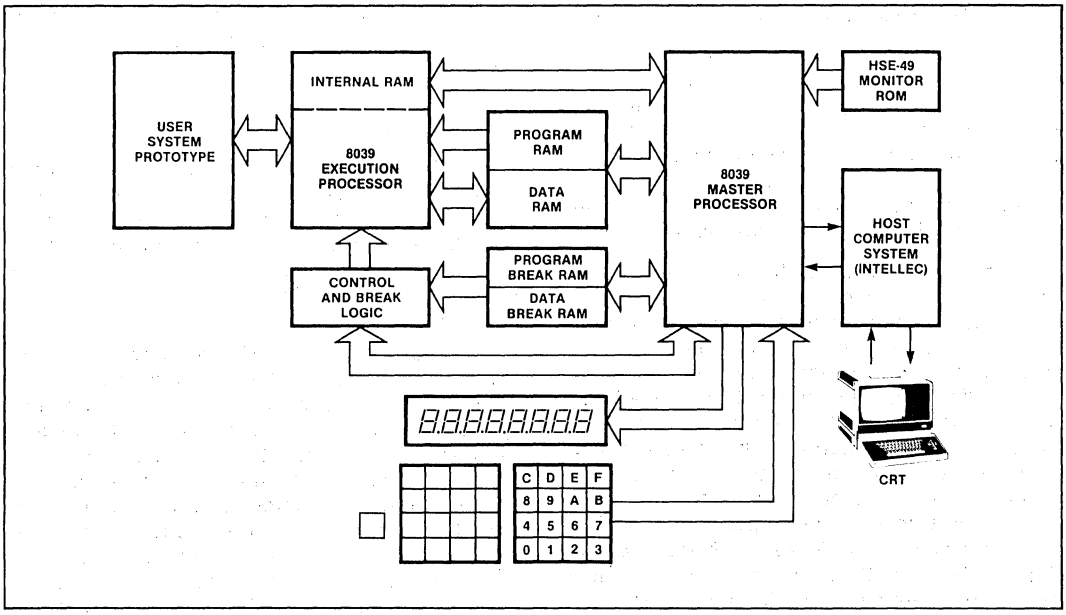


Figure 2. HSE-49 Emulator Signal Flow Diagram

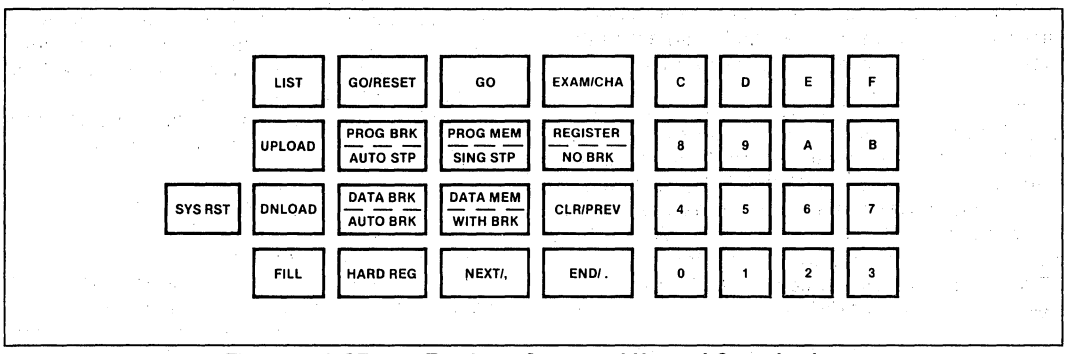


Figure 3. HSE-49 Emulator Command Keypad Organization

ment commands, drive serial interfaces, etc. In general, this master processor (MP) is used to interface the emulation processor's memory spaces with the outside world and control the operation of the EP. Figure 2 shows how the two processors interrelate with the rest of the system. Figure 3 shows the layout of the 33-key keypad through which the user interfaces to the emulator.

MP MONITOR

The monitor program executed by the MP includes commands for filling, reading, or writing the various memory spaces, including the execution processor's program RAM, external ("MOVX") data RAM, accumulator, PSW, PC, timer/counter, working registers, and internal RAM; executing the user's program from arbitrary addresses in various debugging modes; and uploading or downloading object or data files from diskettes using a host development system. No special software is needed for the Intellec system other than ISIS II Version 3.4 or later. The data format is compatible with the standard Intel hex file format produced by ASM-48; the baud rate may be altered from 110 baud (default state) up to 1200 baud from the onboard keypad. Blocks of data may be transmitted to a CRT or printer and displayed in a tabular format.

INTERPROCESSOR COMMUNICATION

An 8212 8-bit latch is used to communicate data and commands between the master and emulation processors. Under control of the MP, this register, call the "Link" register, may be logically mapped into either the program or data RAM address spaces. When this is done, the RAM in the respective memory space is disabled and the link responds to all accesses regardless of address.

When the MP detects that the EP has been halted by the breakpoint hardware, or when the operator presses a key while the program is executing, the program break sequence is initiated. The low-order 23 bytes of user-program memory is read into a buffer within the internal RAM of the MP. A short program for reading and transmitting internal EP status is written into the low-order user-program memory. (This is one of several "mini-monitors" overlayed on the user-program area.) The link register is mapped logically into the user-program memory, and loaded with the 8049 machine code for a "CALL" instruction to the mini-monitor program area. The EP is then allowed to fetch a single instruction from the link, forcing the "CALL" to the mini-monitor onto the EP data bus. The link register is then mapped to the external data RAM address space. A block diagram of the system at this point is shown in Figure 4.

From this point on, the EP executes code contained in the mini-monitor which makes the EP accumulator, timer/counter and PSW values available to the MP (through "MOVX" instructions to the link register) so that the EP internal status may be saved in the MP internal data RAM. The MP then loads a different mini-monitor into the same EP program RAM area which allows it to read and save the internal RAM of the EP.

At this point, the HSE-49 emulator may be interrogated or given instructions by the operator from the hex keypad. The emulator operation remains transparent to the user, who need not be concerned, for example, with the actual (altered) location of the EP low-order program RAM or internal data RAM.

In order to resume user-program execution, a status restoration mini-monitor is overlayed. This restores the EP internal status using a scheme analogous to the one in which the status was originally saved. The final step of the last mini-monitor is an "RETR" instruction, after which the EP is again halted. The low-order program memory saved earlier is rewritten into the appropriate area, the break logic is configured for the desired execution mode, and the EP is released to run at full speed until the next break situation is encountered.

Operation Modes

The HSE-49 firmware is a ROM-based program that provides the user with simple key-stroke commands for initiating emulation, defining breakpoints, and displaying and controlling system parameters. A summary of the HSE-49 emulator commands is given in Table 1.

SIX EMULATION MODES are provided by the HSE-49 emulator to aid in hardware and software debugging. The user may single-step through a program or have the emulator automatically step through the program with a user-defined idle time between steps. Three real-time emulation commands allow 1) real-time emulation with breakpoints not enabled (a user-accessible pulse is generated each time a breakpoint is encountered, however, facilitating user-defined logic analysis), 2) real-time emulation with breakpoints enabled, and 3) real-time emulation with automatic breakpointing, whereby the emulator executes in real time between breakpoints, and pauses at each breakpoint for a user-defined time before automatically resuming real-time emulation. A final command initiates real-time execution, beginning emulation at user-program location 000H, from the Emulator Processor hardware reset state.

BREAKPOINTS may be set at any combination of program memory and external data memory address locations from 000H to FFFH. This unlimited capability to specify breakpoints for all possible combinations of addresses complements the somewhat different breakpointing features available with the ICE-49 emulator.

The ICE-49 emulator permits the symbolic specification of breakpoints on program memory and external data memory addresses, or external data memory address reads or writes individually, and upon the input of an external synchronization signal.

INTERROGATION AND UTILITY commands are provided by the HSE-49 emulator which allow the user to examine, change or fill the various emulator memory spaces. Additional commands are provided to upload or download the contents of the memory spaces to or from a host Intellec development system, or other peripheral device, through the HSE-49 emulator serial port.

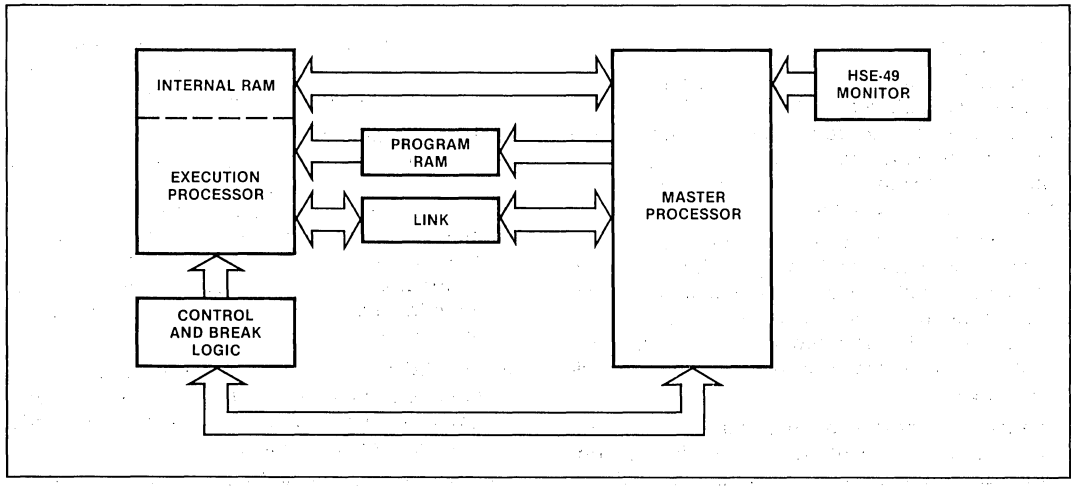


Figure 4. Communication between EP and MP

Table 1. HSE-49 Emulator Command Description

Command	Command Modifier	Description
GO		Begins emulation:
	NO BRK	Real-time breakpoints not enabled
	W/BRK	Real-time breakpoints enabled
	SING STP	Steps program one instruction
	AUTO STP	Automatically steps/pauses/steps/...
	AUTO BRK	Automatically emulates real-time/pauses at breakpoint/emulates real-time/...
GO/RESET	(NONE)	Begins real-time emulation from EP hardware reset state, beginning at program location 000H
B, C	(PROG MEM, DATA MEM)	Sets (B) or Clears (C) breakpoint at specified address within Program or External Data memory
SYS RST	(NONE)	Resets emulation and master processors and clears all breakpoints
EXAM/CHA	*	Examine/Change memory location
FILL	*	Fill range of memory addresses with a single data value
LIST	*	List memory to output device through HSE-49 serial port
DNLOAD	*	Download hex-file format memory to HSE-49 emulator through HSE-49 serial port
UPLOAD	*	Upload memory within a range of addresses through HSE-49 serial port to Intellec Development System or external peripheral device
	*:	* = Memory types allowed for above commands:
	PROG MEM	User-program memory
	DATA MEM	External data memory (if installed)
	PROG BRK	User-program breakpoint memory
	DATA BRK	External data breakpoint memory
	REGISTER	Register memory and internal data memory
	HARD REG	Hardware registers/system control parameters

Limitations

The HSE-49 emulator was not designed to have the same capabilities that Intel's ICE™in-circuit emulators have, and certain features have been deleted to keep the circuitry relatively simple. As a result, the following limitations exist and should be taken into account when using the system.

1. As explained previously, user-program execution is terminated by forcing the EP to execute a "CALL" instruction to the mini-monitor. Because this requires one level of the EP subroutine stack, the user program can be using a maximum of seven levels of stack when a break is initiated.
2. Because program execution is initiated by forcing the EP to execute an "RETR" instruction, the EP interrupt-in-progress flip-flop will be cleared. Therefore, if interrupts are enabled, emulation should not be resumed from an address within an interrupt servicing routine; if it is, the EP may incorrectly recognize an interrupt request which should be ignored.
3. The I/O status of ports P0 and $P2_2$-$P2_3$ with respect to user-supplied hardware is determined by the HSE-49 emulator hardware configuration rather than by software. Therefore the I/O modes of these ports may not be altered while a program is executing. These ports may be configured as is inputs, latched outputs or bidirectional ports by changing socketed HSE-49 emulator hardware.
4. The "ANL BUS, #nn" and "ORL BUS, #nn" instructions may not be used in the user program, as external hardware cannot properly restore these functions.

Several other minor limitations with the HSE-49 emulator operation are explained in the Operating Instructions.

SPECIFICATIONS

Equipment Supplied

Printed Circuit Board with Integral Keypad, Display, ROM Monitor, (2) 8039 microprocessors and 2K bytes user program RAM

Emulation Cable and Plug

Serial-Link Cable

Power Pick-up Card with Cable

Power Cable

Emulation Clock

11 MHz supplied, or user supplied crystal for 3.6 MHz to 11 MHz clock

Serial I/O

20 mA Current Loop or RS232 (jumper selectable)

Physical Characteristics

Width: 14.0 in (35.6 cm)
Length: 10.0 in. (25.4 cm)
Height: 0.5 in. (1.27 cm)
Packaged Weight: 4.0 lb (1.8 kg)

D.C. Electrical Characteristics

V_{CC} = +5V ±5%
I_{CC} = 2.0A max; 1.5A typical
V_{RS232} = +12V ±5%; −12V ±5%
I_{RS232} = 0.020A max; 0.015A typical

(V_{RS232} required only if using RS232 mode of serial port)

Environmental Characteristics

Operating Temperature: 0° to 55°C

Operating Humidity: Up to 90% relative humidity without condensation

ORDERING INFORMATION

Part Number	Description
MCI-49-HSE	8048/8049 family CPU high-speed (11 MHz) emulator, cable assembly and ROM firmware